CREATIVE ELECTRONIC SYSTEMS

# Distributed Computing Goes Safety 3U-VPX Mission Computers

*Embedded Tech Trends*

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## Abstract

The processing architecture in Mission Computer (MC) system is going toward distributed computing allowing system modularity, safety architecture and scalability.

They are two key factors supporting distributed architecture: the continuous improvement of the size, performance and power efficiency of the processors, following Moore's law, and high speed processors communication with protocol such as PCIe. Together with the high number of PCIe controllers on chip, the processors communicate with very low latency, deterministically and making remote processing a snap.

Distributed architecture is providing the foundation for a safety partitioning which is paramount in mission computers. We will show how distributed computing can be applied to 3U-VPX MC for mission safety while ensuring system future proof.

# Top Down Design of COTS Mission Computers

Processing Architecture to make systems:

Customizable

Modular

Safety Critical

Scalable

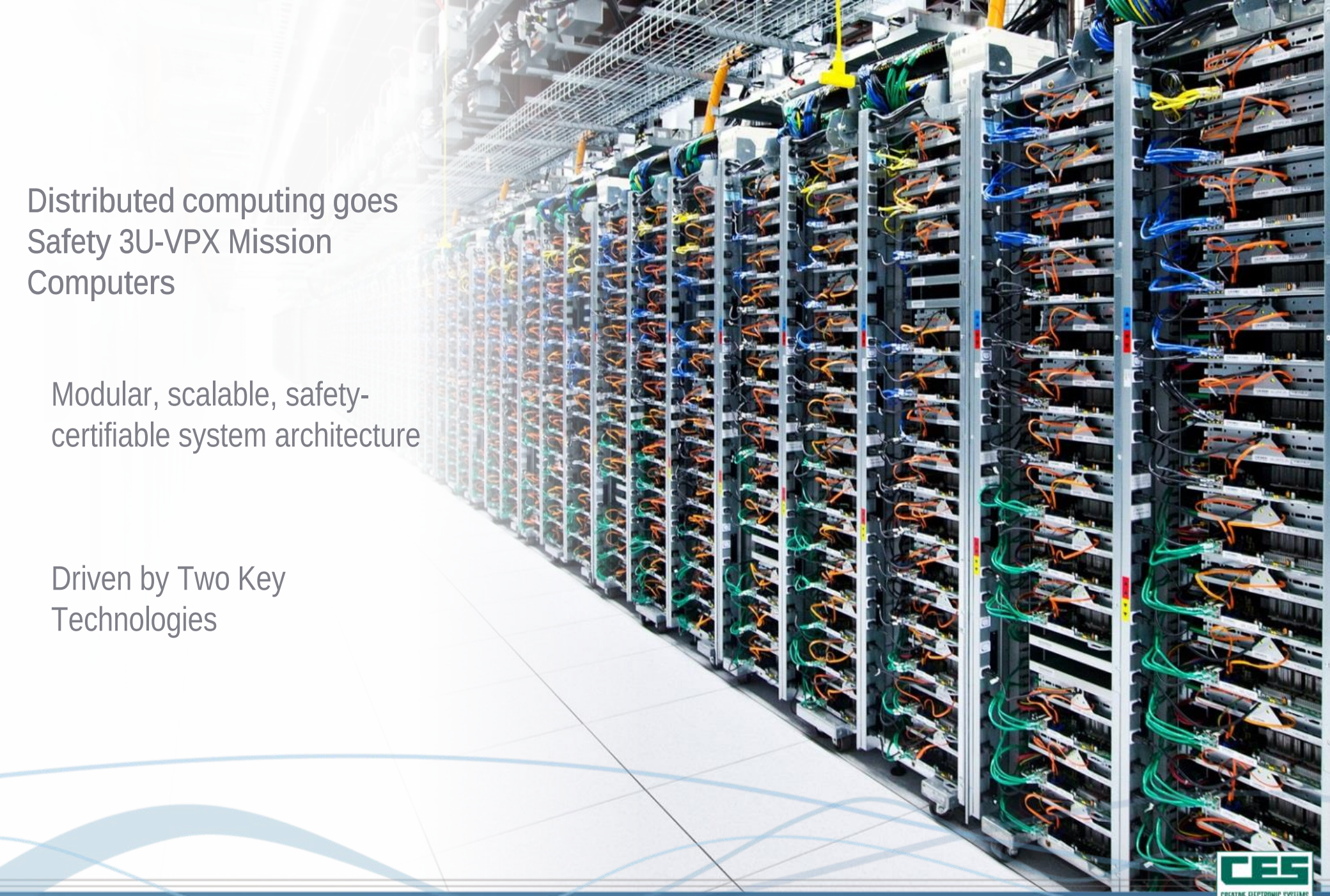
# 3U-VPX COTS Mission Computer: Definition

Prequalified for harsh environmental conditions
Full features for C4ISR Mission Applications
Optimized SWaP
Certifiable for Safety
Customizable
Future proof architecture

# Distributed computing goes Safety 3U-VPX Mission Computers

Modular, scalable, safety-certifiable system architecture

Driven by Two Key Technologies

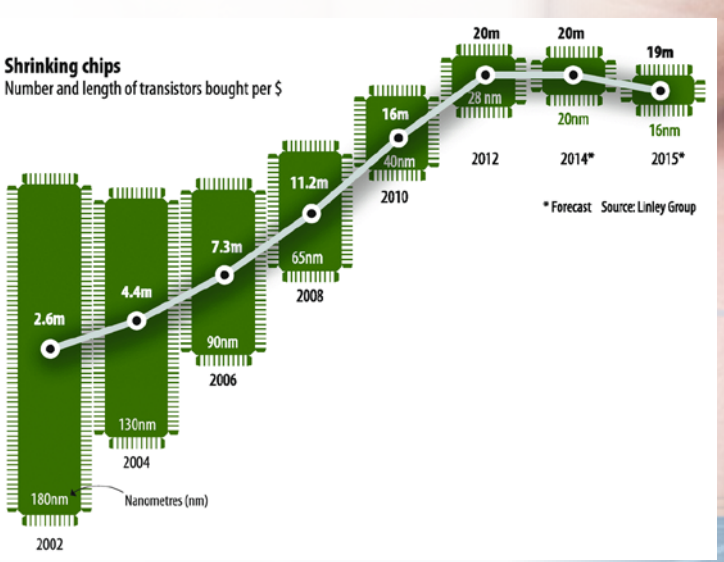


# Tech #1: SOC Technology Trend

Announcing 14nm products and going down

Leading to ultra small but powerful processing nodes

Highly Connected: SERDES controllers, accelerators, embedded buffer



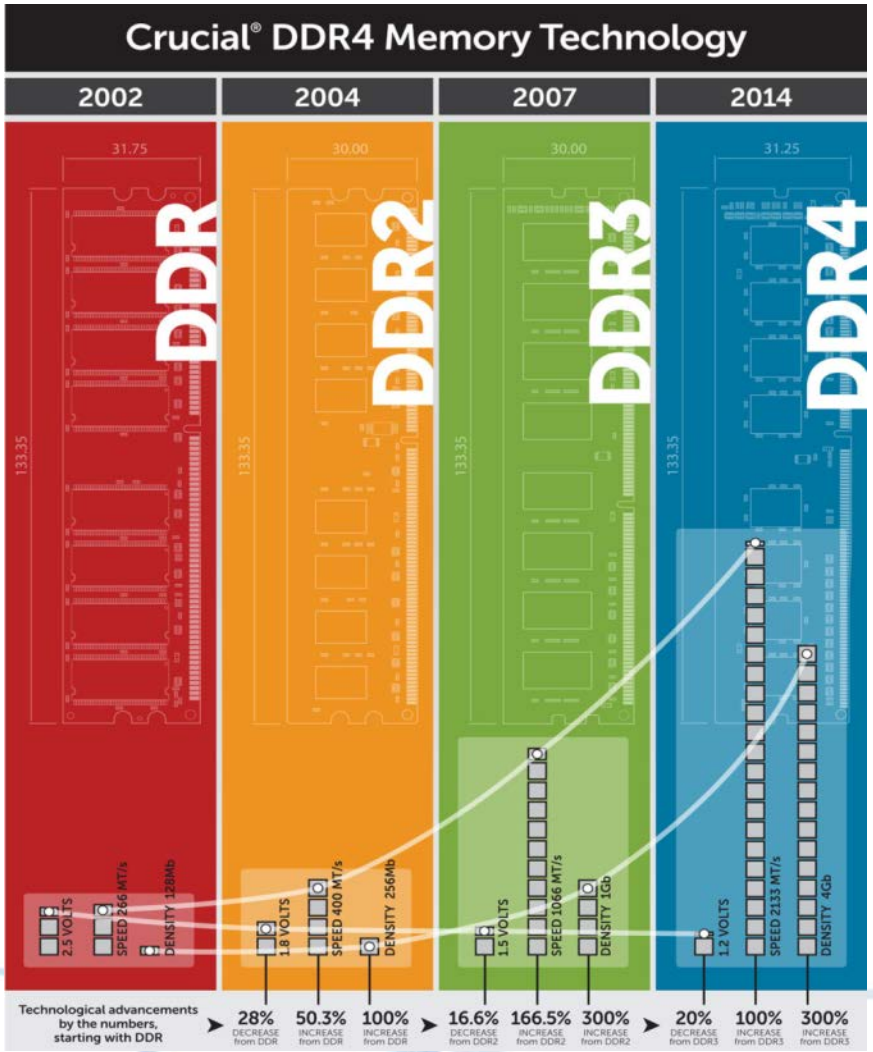
# Tech #2: Interconnect Speed

Fast network data pipe and getting faster

PCIe connection:  Low Latency, no overhead, atomic operation

Examples:
Gen3, x8 = 16GBps – No latency
64bit DDR3@1600 = 12.8GBps + Overhead

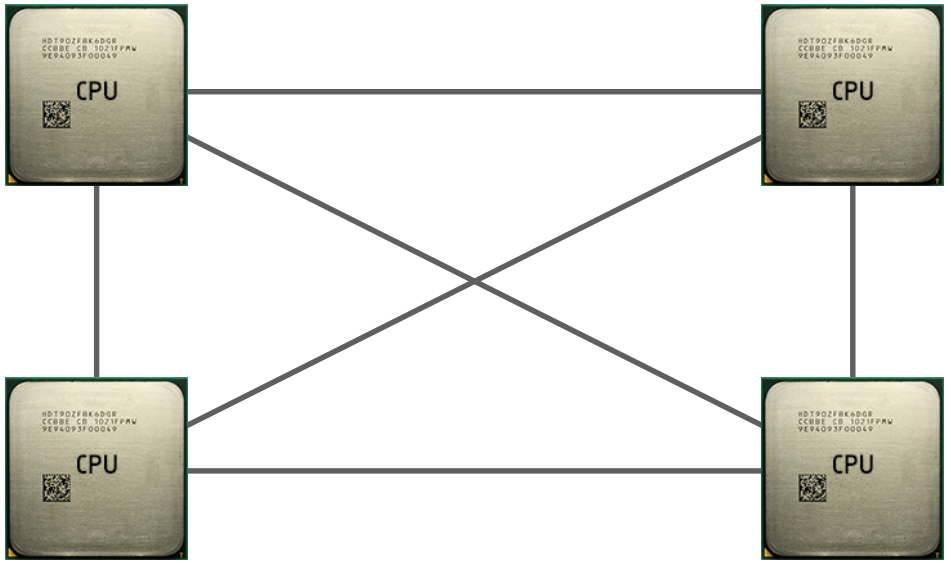
| | Raw Bit Rate | Link BW | BW/Lane/Way | Total BW x16 |
|---|---|---|---|---|
| PCIe 1.x | 2.5GT/s | 2Gb/s | ~250MB/s | ~8GB/s |
| PCIe 2.x | 5.0GT/s | 4Gb/s | ~500MB/s | ~16GB/s |
| PCIe 3.x | 8.0GT/s | 8Gb/s | ~1GB/s | ~32GB/s |
| PCIe 4.0 | 16GT/s | 16Gb/s | ~2GB/s | ~64GB/s |



# Make The Connection: Full Mesh Network

*The processors communicate with very low latency, deterministically and making remote processing a snap*

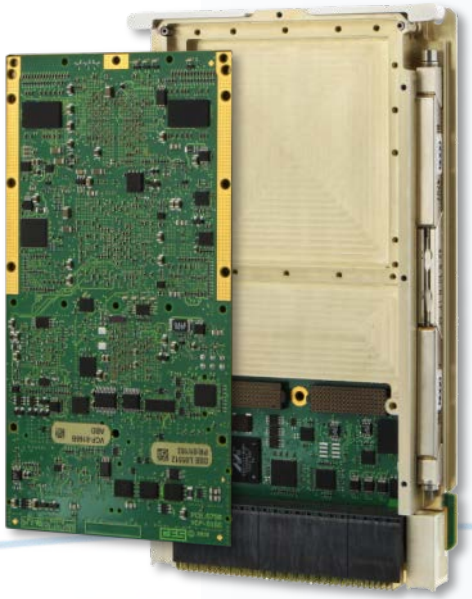
- Fully deterministic
- Safety friendly
- Segregation of different DAL level
- Lowest latency



# Time for a flip

IOs Rich functions on board

Processor on Mezzanine



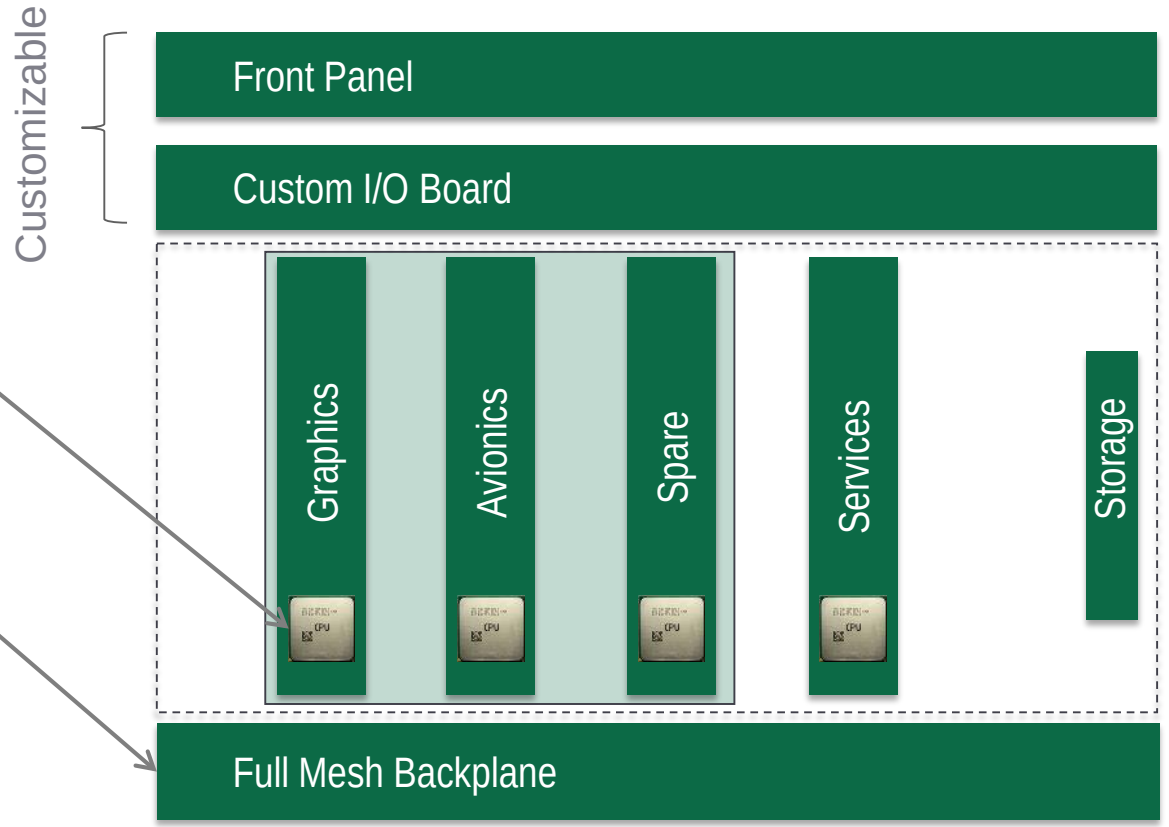
# COTS 3U-VPX ARCHITECTURE

## Distributed Computing

Processors on Mezzanines
Easy Processors Upgrade

Full Mesh Back plane

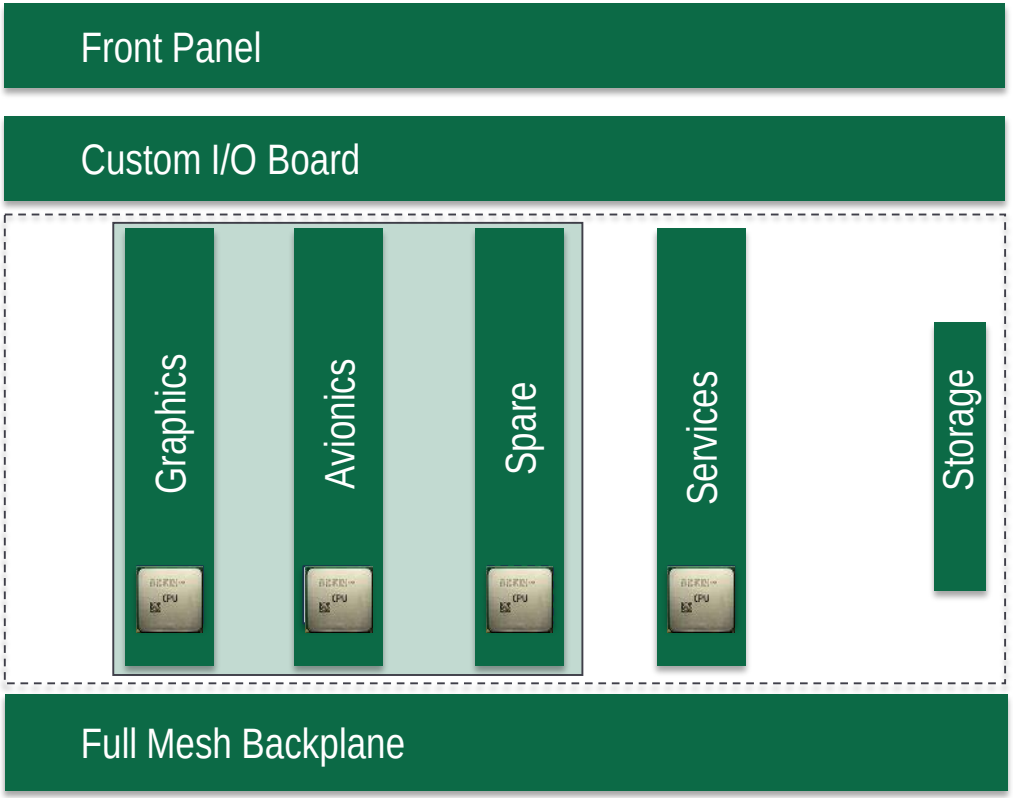
Modularity

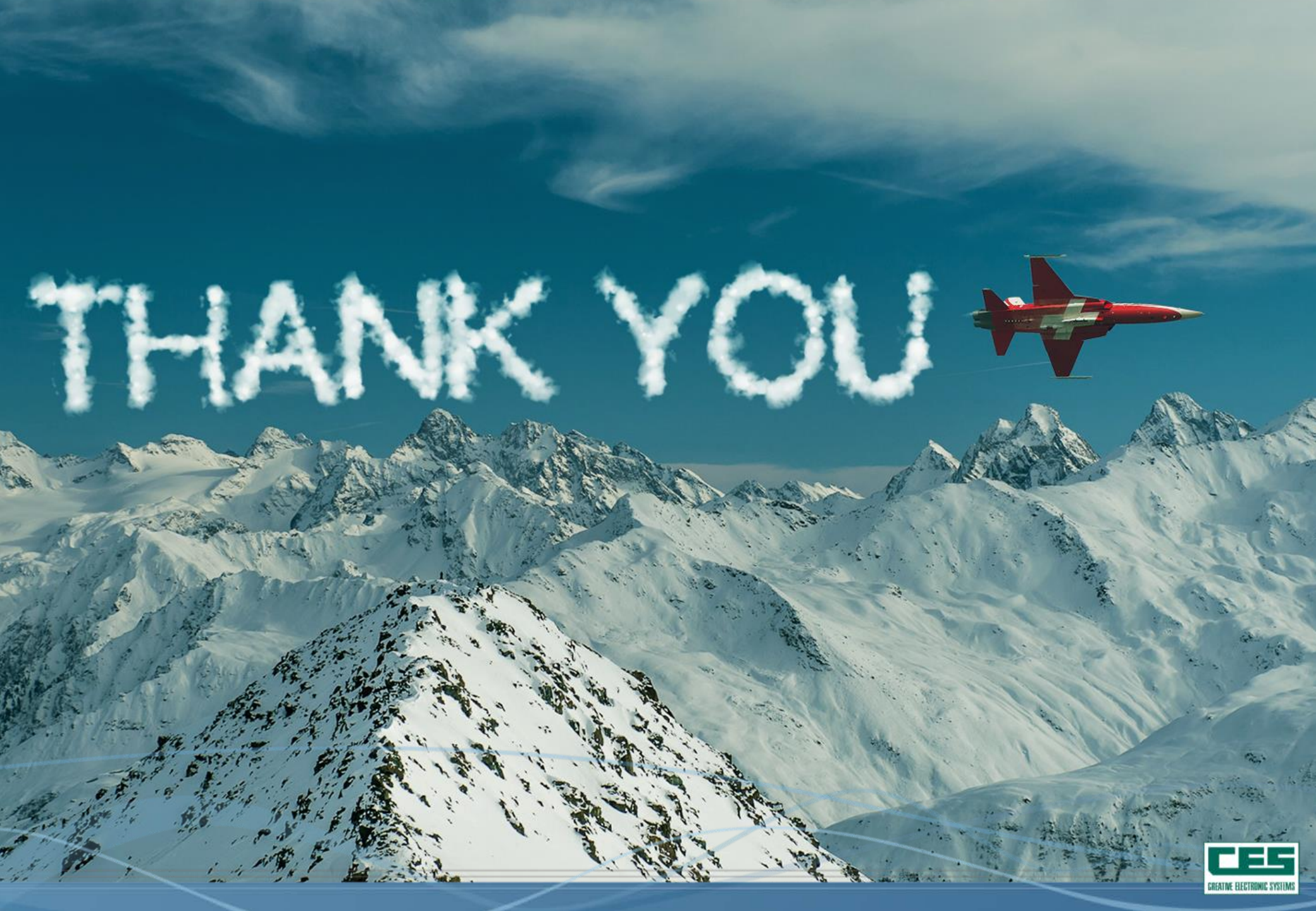


# Next Generation CES COTS Mission Computer

## Advantages

- Scalable 1-4 Multi-Cores Processors
- Safety Support with Segregation and mixing DAL levels
- SWaP optimized
- Future Proof Architecture




THANK YOU
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